IN THE CLAIMS

Please cancel claims 22 and 26, amend claims 1, 19 and 25, and add new claims 28-32 as follows:

1. (CURRENTLY AMENDED) A conditional access module, configured to control access to a media program via a receiver communicably coupleable to the conditional access module, comprising:

a first processor;

a second processor; and

an interface module, communicatively coupled to the first processor and the second processor, the interface module configured to process all communications with the conditional access module and to externally manifest a single virtual processor to the receiver;

wherein the interface module receives messages from the receiver, interprets the received messages, and generates first processor messages for the first processor and second processor messages for the second processor, the first processor messages and the second processor messages defining a functional allocation between the first processor and the second processor and wherein the received messages include encrypted data and the functional allocation is time varied according to the encrypted data.[[.]]

2. (ORIGINAL) The apparatus of claim 1, wherein the first processor performs a subset of functions to control access to the media program and the second processor performs a second subset of functions to control access to the media program.

3. (ORIGINAL) The apparatus of claim 1, wherein:

the first processor is communicatively coupled a first processor memory;

the second processor is communicatively coupled to a second processor memory; and

wherein the first processor memory is isolated from the second processor and the second processor memory is isolated from the first processor.

4. (PREVIOUSLY PRESENTED) The apparatus of claim 1, wherein the interface module comprises:

a first module configured to receive conditional access module messages; and

a second module configured to interpret the received messages and configured to generate first processor messages for the first processor and second processor messages for the second processor from the received messages.

5. (PREVIOUSLY PRESENTED) The apparatus of claim 4, wherein the interface module comprises:

a third module configured to receive a first set of response messages generated by the first processor and a second set of response messages generated by the second processor; and

a fourth module configured to generate conditional access module response messages using at least a portion of the first set of response messages and at least a portion of the second set of response messages.

6.-10. (CANCELED)

11. (PREVIOUSLY PRESENTED) The apparatus of claim 1, wherein the interface module receives a first set of response messages generated by the first processor and a second set of response messages generated by the second processor and generates conditional access response messages using at least a portion of the first set of response messages and at least a portion of the second set of response messages.

12. (PREVIOUSLY PRESENTED) The apparatus of claim 1, wherein the interface module is a processor.

13. (PREVIOUSLY PRESENTED) The apparatus of claim 1, wherein the interface module is a hardware state machine.

14. (ORIGINAL) The apparatus of claim 1, wherein the first processor and the second processor are communicatively coupled to a shared charge pump.

15. (PREVIOUSLY PRESENTED) The apparatus of claim 1, wherein the first processor and the second processor are communicatively coupled to a shared programming control module, the shared program control module external to the interface module.

16. (ORIGINAL) The apparatus of claim 1, wherein the first processor and the second processor each include it's own separate components selected from the group comprising:

voltage supply;

clock;

coprocessor;

read only memory; and

random access memory.

17. (ORIGINAL) The apparatus of claim 1, wherein the first processor and the second processor include separate logical address ranges.

18. (ORIGINAL) The apparatus of claim 1, wherein the first processor and the second processor include separate physical address ranges.

19. (CURRENTLY AMENDED) A method of controlling access to a media program, comprising the steps of:

receiving a message in a conditional access module from a receiver, the message comprising encrypted information to be decrypted by operations independently performed by a both a first processor and a second processor in the conditional access module;

generating first processor commands and second processor commands from the message;

providing the first processor commands to the first processor and the second processor commands to the second processor;

receiving a first processor response from the first processor;

receiving a second processor response from the second processor; and

generating a conditional access message response from at least a portion of the first processor response and the second processor response;

wherein the media program is encrypted by a control word, the encrypted information is a control word packet, and the conditional access message response is the control word and wherein the first processor messages and the second processor messages define a functional allocation between the first processor and the second processor and wherein the functional allocation is time varying.

20. (CANCELED)

21. (ORIGINAL) The method of claim 19, wherein first processor and the second processor operate independently and wherein the step of generating first processor commands and second processor commands from the message comprises the steps of:

alternately directing received messages to the first processor and the second processor.

22. (CANCELED)

23. (ORIGINAL) The method of claim 22, wherein the functional allocation is time varied according to a clock received externally from the conditional access module.

24. (ORIGINAL) The method of claim 22, wherein the received messages include encrypted data and the functional allocation is time varied according to the encrypted data.

25. (CURRENTLY AMENDED) An apparatus configured to control access to a media program, comprising:

means for receiving a message in a conditional access module from a receiver, the message comprising encrypted information to be decrypted by operations independently performed by a both a first processor and a second processor in the conditional access module;

means for generating first processor commands and second processor commands from the message;

means for providing the first processor commands to the first processor and the second processor commands to the second processor;

means for receiving a first processor response from the first processor;

means for receiving a second processor response from the second processor; and

means for generating a conditional access message response from at least a portion of the first processor response and the second processor response;

wherein the media program is encrypted by a control word, the encrypted information is a control word packet, and the conditional access message response is the control word and wherein the first processor messages and the second processor messages define a functional allocation between the first processor and the second processor and wherein the functional allocation is time varying.

26. (CANCELED)

27. (PREVIOUSLY PRESENTED) The apparatus of claim 15, wherein the shared programming control module is configured to synchronize common data stored in the first processor and the second processor.

28. (NEW) The apparatus of claim 1, wherein the interpreted message includes encrypted data, and wherein first processor partially decrypts the encrypted data and the second processor further decrypts the partially decrypted data.

29. (NEW) The apparatus of claim 28, wherein the partially decrypted data is provided from the first processor to the second processor via the interface module.

30. (NEW) The apparatus of claim 28, wherein the partially decrypted data is provided directly from the first processor to the second processor.

31. (NEW) The apparatus of claim 1, wherein the first processor and the second processor perform a decryption operation comprising a set of functions that are allocated to the microprocessor or the second microprocessor.

32. (NEW) The apparatus of claim 31, wherein multiplication functions are assigned to the first processor and addition functions are assigned to the second processor.